CLAIMS

What is claimed is:

1. A method of forming a conductive line on a semiconductor wafer, the method comprising:

forming a trench on the semiconductor wafer;

depositing a dielectric material in the trench so that a hollow enclosed conduit is formed within the dielectric material in the trench; and

forming at least one via hole in the dielectric material deposited in the trench and configured to intersect the hollow enclosed conduit; and

filling the hollow conduit by using the at least one via hole to thereby form the conductive line.

2. The method of forming a conductive line as recited in claim 1, wherein the hollow conduit is filled with a conductive material.

3. The method of forming a conductive line as recited in claim 2, wherein the conductive material is one of Ti, TiN, W, Al, Cu, and Mb.

4. The method of forming a conductive line as recited in claim 1, wherein the deposition of the dielectric material is controlled so that the top part of the enclosed conduit is formed by mushrooming of the overhang on the sides of the trench.

5. The method of forming a conductive line as recited in claim 1, wherein the trench is formed by etching one of a silicon substrate of the semiconductor wafer or an oxide layer formed on the wafer.

6. The method of forming a conductive line as recited in claim 1, wherein the trench is formed by at least two prominences on a patterned layer on the wafer.

7. The method of forming a conductive line as recited in claim 6, wherein at least one of the at least two prominences comprises an interconnect line.

8. The method of forming a conductive line as recited in claim 1, wherein the filling the hollow conduit comprises one of a chemical vapor deposition, plasma enhanced chemical vapor deposition, and atomic layer deposition method.

9. The method of forming a conductive line as recited in claim 1, wherein the depositing the dielectric in the trench comprises one of a chemical vapor deposition and physical vapor deposition method.

10. The method of forming a conductive line as recited in claim 2, wherein the conductive line is configured in a spiral shape to form an inductor.

11. The method of forming a conductive line as recited in claim 2, wherein the conductive line forms a fusible link in a circuit.

12. The method of forming a conductive line as recited in claim 2, wherein the conductive line is hollow and further comprising filling the hollow conductive line with a dielectric material in an annular shape and filling the space defined by the annular shape with a conductive material to form a second conductive line.

13. The method of forming a conductive line as recited in claim 12, wherein the first and second conductive lines form a coaxial conductor

14. The method of forming a conductive line as recited in claim 2, wherein the trench has an aspect ratio greater than or equal to 1.

15. The method of forming a conductive line as recited in claim 1, wherein the at least one contact hole comprises a plurality of contact holes and wherein the adjacent of the plurality of contact holes are positioned less than a predetermined maximum fill distance length apart.

16. The method of forming a conductive line as recited in claim 1, wherein the conductive line is configured to form one of a fuse, an interconnect, a resistor, a capacitor, and an inductor.

17. A method of forming a signal transmission line on a semiconductor wafer, the method comprising:

forming a channel within a first layer on the semiconductor wafer;

depositing a dielectric material in the channel, wherein the dielectric material and the channel configurations are selected so that a hollow enclosed conduit is formed in the channel;

forming at least one via hole in the dielectric material deposited in the channel and configured to intersect the hollow enclosed conduit; and

filling the via hole and the hollow enclosed conduit with a first material to thereby form the signal transmission line, whereby the first material is one of a dielectric and a conductor.

18. The method of forming a signal transmission line as recited in claim 17, wherein the first material is a dielectric configured for transmitting optics.

19. A semiconductor integrated circuit formed by:

forming a channel within a first layer on a semiconductor wafer;

depositing a dielectric material in the channel, wherein the dielectric material and the channel configurations are selected so that a hollow enclosed conduit is formed in the channel;

forming at least one via hole in the dielectric material deposited in the channel and configured to intersect the hollow enclosed conduit; and

filling via hole and the hollow enclosed conduit with a first conductive material to form a conductive metal line.

20. The semiconductor integrated circuit of claim 19 wherein the conductive metal line is configured in a spiral shape to form an inductor.

21. The semiconductor integrated circuit of claim 19 wherein the conductive metal line is configured to form one of a fusible link, resistor, capacitor, and interconnect line.